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Research Article

The implementation of ozone cleaning on two-step texturization of p-type silicon wafer

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Abstract. This study investigates the ozone treatment process that can be utilized across various fabrication stages to enhance the performance of silicon solar cells. The effectiveness of this treatment on p-type silicon surfaces was examined through the application of ozone dissolved in deionized water (DIO_3) and the ultraviolet-ozone (UVO_3) cleaning process prior to the two-step texturization procedure. The two-step texturization procedure applied in this work eliminates the use of silicon nitride (SiN) as an anti-reflective coating (ARC) layer for the elimination of toxic gases and leads to the environment-friendly fabrication of solar cells. An alternative to RCA, DIO_3 and UVO_3 represent promising chemical options for cleaning applications to eliminate the use of hazardous chemicals. It was discovered that the surface with the DIO_3 treatment for 10 minutes resulted in a significantly enhanced surface quality on the p-type silicon wafer. In the DIO_3 cleaning, ozone is dissolved in deionized water to create a highly oxidative solution capable of removing organic contaminants and particles effectively. In contrast, the UVO_3 treatment harnesses ultraviolet light to synthesize ozone directly on the wafer's surface, promoting the degradation of organic residues into volatile compounds, including CO_2 and H_2O. According to field emission scanning electron microscope (FESEM) micrographs and UV-visible spectrometer (UV-Vis) measurements, the textured wafer with DIO_3 treatment improves the surface morphology and decreases the front surface reflection. As a result, the 10 minutes DIO_3 treatments were reported optimal; the range size and height of the pyramid formed were 1.9–2.0 µm and 0.8–1.5 µm, offering a lower reflectivity value of below 12%, respectively. Results from the Atomic Force Microscope (AFM) also confirm that the increase in average surface roughness from 203.65 nm to 300.27 nm was expected to improve light absorption. Moreover, this methodology leads to a considerable reduction in surface damage and is applicable to the silicon texturization process utilized in solar cell manufacturing.

Keywords: DIO_3 treatment, two-step texturization, p-type wafer, surface morphology, reflectance

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1. Introduction

The efficiency of a solar cell is a crucial attribute, as it directly influences the cell's ability to produce electrical power. Therefore, there is a significant demand for techniques that not only increase the efficiency of solar cells but also refine the manufacturing processes associated with their production (Oni *et al.,* 2024). The modification of the pre-texturization process not only prepares the silicon wafer for efficient texturization but also improves the overall manufacturing process by enhancing surface cleanliness, morphology, and hydrophilicity while reducing environmental impact. These improvements collectively lead to higher-quality solar cells with improved performance and manufacturing efficiency. The modification of the pre-texturization process on the silicon (Si) wafer presented in this study specifically improves surface properties such as reduced surface roughness and enhanced uniformity, which contribute to better light trapping and minimized carrier recombination. Additionally, optical properties such as increased reflectance reduction and optimized light absorption are achieved, thereby improving the overall manufacturing process and performance of Si solar cell architectures.

The pursuit of developing solar cells with enhanced efficiency, simplified manufacturing processes, and reduced costs is an ongoing endeavor (Panagoda *et al.,* 2023). Achieving this objective requires optimizing every step of the production process. Surface cleaning plays a pivotal role in device performance. Thorough cleaning is essential for eliminating dust, contaminants, particles, organic and inorganic impurities, and native oxides from the wafer surface, which ensures optimal device functionality. A variety of cleaning methods are available, broadly categorized into wet chemicals (C. L. Chu *et al.*, 2020; Kart *et al.,* 2018) and dry-cleaning techniques (Neutens *et al.,* 2018). Wet chemical cleaning has been the cornerstone of wafer preparation for decades, with the Radio Corporation of America (RCA) clean recognized as the principal method in the microelectronics sector (Kern & Puotinen, 1970; Ruzyllo *et al.,* 1990). This technique, while highly effective, involves the use of multiple hazardous chemicals such as NH_4OH and H_2O_2. To address environmental and economic concerns, alternatives such as IMEC-Clean have been introduced, which optimize

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chemical usage while maintaining high cleaning efficiency (W. Chen *et al.,* 1997). Among wet chemical methods, DIO_3 has gained prominence due to its strong oxidizing properties and ease of generation through dielectric barrier discharge (G. Chen, 1999; Moldovan *et al.,* 2013; Zou *et al.,* 2021). Studies have highlighted its effectiveness in removing contaminants and preparing wafer surfaces for subsequent processing (Epelle *et al.*, 2023). However, despite the proven advantages of wet cleaning methods, their reliance on large volumes of chemicals and water raises concerns about sustainability and compatibility with next-generation manufacturing technologies. To overcome these limitations, dry cleaning techniques have emerged as complementary or alternative methods. One notable approach is the UVO_3 process. The UVO_3 method combines UV radiation with molecular oxygen to produce reactive species such as ozone (O_3) and atomic oxygen. These species oxidize and decompose organic residues into volatile byproducts like CO_2 and H_2O, effectively removing contaminants without the use of liquid chemicals. The term photosensitized oxidation describes the chemical reactions initiated by UV radiation in the presence of oxygen, leading to the formation of highly reactive species such as singlet oxygen and ozone. These species facilitate efficient cleaning, making the UVO_3 process an environmentally friendly and effective solution. First reported by Bolon and Kunz in 1972, the UVO_3 process has since been demonstrated to improve wafer surface morphology, enhance transmittance, and promote the overall quality of films in applications such as organic photovoltaics (Bolon & Kunz, 1972; Li *et al.*, 2023). By integrating both wet and dry-cleaning techniques into a unified cleaning strategy, it is possible to harness their respective advantages, addressing both the environmental and technological demands of modern silicon wafer processing.

Various texturing techniques have been developed to create pyramid-like structures on Si wafers, each with distinct mechanisms and implications for surface morphology and optical properties. For example, electrochemical etching relies on applying an electrical current to selectively remove silicon, offering precise control over texture but requiring complex setups and stringent conditions (Menna *et al.,* 1995). Metal-assisted chemical etching (MACE) involves the use of metal catalysts to enhance Si dissolution, allowing the formation of high-aspect-ratio structures. However, its dependence on hazardous chemicals can pose environmental and handling challenges (Fang *et al.,* 2008). Physical dry etching, such as plasma etching, physically removes material through ion bombardment, enabling fine control over texture but often at the expense of slower processing rates and higher costs (Garnett & Yang, 2010). The discussion from general texturing methods to those used in industrial applications is important to consider scalability and cost-effectiveness. In the context of industrial-scale solar cell manufacturing, texturization methods primarily employ chemical etching due to their scalability and cost-effectiveness. Conventional methodologies typically utilize alkaline etching solutions, such as isopropyl alcohol (IPA), potassium hydroxide (KOH), and deionized water (DI), to create pyramid-like structures on the Si surface (Chuchvaga *et al.,* 2020; Montesdeoca-Santana. *et al.,* 2013). These solutions exploit the anisotropic etching properties of Si, preferentially dissolving certain crystallographic planes to form pyramids. The outcomes of these industrial processes are strongly influenced by the underlying texturing parameters. Under standard conditions, the resulting pyramid sizes are approximately 2 μm (Jiang *et al.,* 2015). However, variations in process parameters, including etching time, temperature, and chemical concentration, can yield pyramid sizes ranging from 2 μm to 8 μm. This is with corresponding reflectivity values between 14% and 15%. The structured surface produced by pyramid texturing enhances light absorption through numerous internal reflections, reducing reflectivity by approximately 20% compared to flat surfaces. This reduction in reflectivity, along with improvements in carrier lifetime, is closely tied to the size, distribution, and uniformity of the pyramids (Ju *et al.,* 2016). Thus, the transition from general texturing methods to industrial processes emphasizes the need for balancing scalability, environmental considerations, and the optimization of pyramid-textured surfaces to improve solar cell performance.

This study investigates the application of cleaning techniques using DIO_3 and UVO_3, newly integrated with a two-step texturing method, to improve the textural properties of Si wafers while reducing costs, processing time, and chemical usage. The two-step texturing procedure begins with 60 cyclic voltammetry (CV) cycles, a technique involving repeated cycling of the electrode potential to promote controlled surface modification. These cycles assist in forming an initial nano-textured surface by selectively removing material and enhancing the silicon's readiness for the subsequent alkaline etching process. This is followed by a standard alkaline texturing step utilizing KOH and IPA, which generates micro-scale pyramidal structures to enhance light trapping. As detailed in prior research (Norizam *et al.,* 2024), the optimized process effectively combines nano- and micro-scale texturing to achieve superior light absorption characteristics. In this study, five cleaning durations for both DIO_3 and UVO_3 treatments were tested to identify the optimal conditions for texturization. The results demonstrated that ozone-based cleaning not only enhanced the efficiency of the texturing process but also led to a significant reduction in reflectance. The baseline reflectance of the p-type Si wafer was approximately 30%, and the DIO_3 and UVO_3 treatments reduced reflectance by 40-45% relative to the baseline value, achieving reflectance values as low as 16-18%. Moreover, the ozone-based cleaning and texturing approach emphasizes cost-effectiveness. It also reduces chemical consumption by minimizing the need for additional cleaning agents while also shortening processing times compared to conventional methods.

2. Method

2.1 Cleaning and texturization of p-type silicon wafers

A p-type monocrystalline Si wafer, sourced from Nexolon Company, was utilized in this study. The wafer exhibits a thickness of approximately 200 μm and a resistivity ranging from 0.5 to 3.0 Ωcm. The wafers, measuring 20 mm × 20 mm, were subjected to advanced cleaning processes DIO_3 and UVO_3 with the primary objective of optimizing surface preparation for subsequent texturization. By removing organic and inorganic contaminants, native oxides, and particles, these cleaning methods aim to improve the uniformity and quality of the textured surface, ultimately enhancing the optical and electrical performance of the wafers. For the UVO_3 cleaning procedure, a Jelight 42 UV-ozone generator was employed to produce ozone and generate oxide on the wafer surface. The samples were exposed to the generator for intervals of 5, 10, 15, 20, and 25 minutes on each side. The samples were then immersed in a 5% acid hydrofluoric (HF) solution by volume to remove the oxide layer formed during the UVO_3 process. In the DIO_3 cleaning procedure, the samples were immersed in deionized water (BiOLUX Hydrogen Fountain) containing dissolved ozone at a concentration of approximately 4.0 ppm, maintained at ambient temperature. The immersion durations were also set to 5, 10,

15, 20, and 25 minutes, followed by rinsing in deionized water for 1 minute and drying using a nitrogen (N_2)-based dryer.

Following the completion of the cleaning procedure, the texturing process was executed using CV treatment, followed by the application of an alkaline solution. The CV treatment was conducted utilizing an Autolab potentiostat/galvanostat (Metrohm, Model: PGSTAT 204) integrated into a three-electrode electrochemical setup. In this configuration, the Si sample acted as the working electrode, platinum served as the counter electrode, and a standard Ag/AgCl (3M KCl) electrode was used as the reference electrode. The choice of a 0.5M Na_2SO_4 electrolyte at approximately pH ~7 was based on its stability, non-reactivity with the Si substrate, and ability to support consistent electrochemical cycling. The potential range of -1.0 to 1.0 V (vs. Ag/AgCl) and the sweep rate of 0.1 V/s were selected to balance the uniformity of surface modification and process duration, as reported in prior studies (Norizam *et al.,* 2024). A total of 60 voltammetric cycles were performed, as this number was optimized based on a combination of surface morphology, reflectivity, and carrier lifetime results in earlier research. The alkaline texturing process involved mixing KOH, IPA, and DI water in a ratio of 1:5:125. This specific ratio was selected since it promotes the formation of uniform micro-sized pyramidal structures by balancing the etching rate and maintaining surface wettability. The reaction temperature was maintained at 70°C, ensuring a consistent etching process without inducing excessive surface roughness. The reaction duration was set to 30 minutes to achieve optimal pyramid formation while minimizing over-etching or material degradation. The resultant surface texturing significantly enhances light absorption due to the reduction in reflectivity caused by the micro-pyramids.

2.2 Morphological and optical properties characterization of p-type silicon wafers

The morphology of the textured samples was examined utilizing FESEM with a Zeiss SUPRA 55 VP instrument. Additionally, FESEM was employed post-texturing to analyze the cross-sectional images and to quantify the height and average dimensions of the pyramidal structures resulting from various cleaning duration followed by the two-steps texturization process. The topographic images obtained through AFM were captured in tapping mode utilizing the AFM Nanosurf Easyscan 2. This system is an atomic force microscope capable of measuring the topography of samples along with various other properties at a resolution on the nanometer scale. The surface reflectance of each sample was examined using a UV-Visible Spectrometer (Model: LAMBDA 35) in the wavelength spectrum of 400-700 nm. Subsequently, structural characterization was performed using an X-Ray Diffractometer (XRD) (Bruker, D8 Advance).

3. Results and discussion

3.1 Surface roughness analysis

The process of surface cleaning aims to eliminate all forms of dust, contaminants, particles, and both organic and inorganic impurities, as well as native oxides from the wafer surface. This procedure is critical for device performance, as thorough cleaning ensures optimal quality and functionality. To assess the impact of ozone treatment and subsequent cleaning procedures, AFM analysis was conducted to evaluate key surface characteristics, including surface roughness, morphology, and

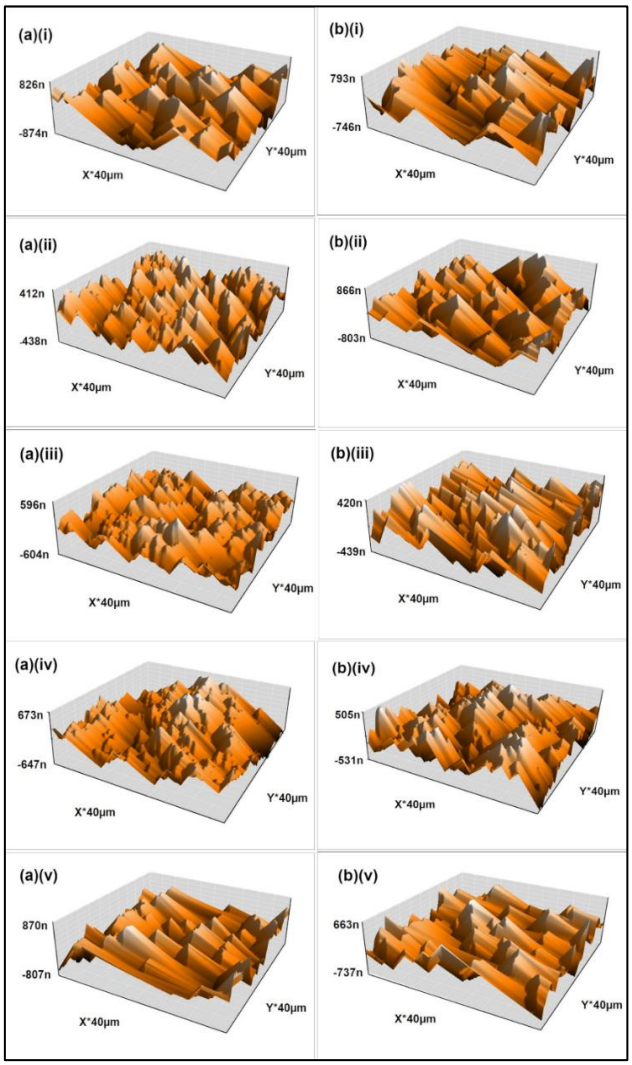

Fig 1. AFM images of (a) DIO_3 and (b) UVO_3 cleaning process for (i) 5, (ii) 10, (iii) 15, (iv) 20 and (v) 25 minutes exposure time

potential residual contamination levels on the Si wafer. The AFM images were recorded following the two-step texturing procedure, providing detailed insights into the nanoscale surface structure and uniformity of the wafer. A clean wafer surface plays a pivotal role in enhancing the effectiveness of the texturing process. By removing impurities and ensuring a uniformly smooth surface, the interaction between the wafer and the texturing solution becomes more predictable, leading to more uniform and well-defined texturing patterns. This improvement is expected to result in reduced reflectivity, better light trapping capabilities, and increased carrier lifetime, all of which contribute to the overall performance and efficiency of the Si wafer in solar cell applications.

Fig 1 (a) and (b) display the AFM images of DIO_3 and UVO_3 treatments across five distinct exposure durations, respectively. The AFM images illustrate that the application of ozone cleaning prior to the texturing process results in optimal surface roughness, which is essential for the effective performance of solar cells. The DIO_3 cleaning process, characterized by a 10-minutes immersion period, results in a superior rough surface, as illustrated in Fig 1 (a)(ii). In contrast, the UVO_3 exposure requires a longer duration, as displayed in Fig 1 (b)(iv), to achieve an optimized rough surface that minimizes reflection effectively.

Fig 2 illustrates the changes in the average roughness of the Si surface in relation to the exposure to UVO_3 and DIO_3, as well as the duration of immersion. The optimal average roughness of 300.27 nm was attained after a 10-minutes immersion in DIO_3. The data presented in Fig 2 indicate that following immersion treatment in DIO_3 for durations of 15, 20, and 25 minutes, the average roughness values decrease to 252.19 nm, 219.68 nm, and 203.65 nm, respectively. The data indicate that the rate of decrease in average roughness is more pronounced during the 15–25-minutes interval when compared to the period prior to 10 minutes.

Consequently, the efficiency of contaminant removal is significantly higher in the initial 10 minutes than in the subsequent time frame. The UVO_3 treatment illustrated in Fig 2 indicates that the optimal average roughness is attained after an exposure duration of 20 minutes. The average roughness for exposure of 5, 10, and 15 minutes was 183.11 nm, 234.83 nm and 240.49 nm, respectively. Subsequent exposure beyond the 20-minutes mark results in a decrease in average roughness (247.51 nm) compared to the measurements taken prior to this time interval. As a result, it can be inferred that the UVO_3 treatment represents a more time-intensive cleaning procedure for applications involving solar cells.

Both UVO_3 and DIO_3 treatments result in the formation of a thin Si oxide layer on the Si surface. This oxide layer serves to passivate the surface, thereby diminishing recombination sites, which is beneficial for solar cell performance (M. Chu *et al.,* 2024). In the initial phases of UVO_3 or DIO_3 treatment, the growth of the oxide can induce localized discrepancies in surface morphology. Such roughness may arise from varying oxidation rates across the Si surface, often influenced by inherent defects or the initial atomic-scale roughness. During the early treatment stages, the oxidation process occurs relatively rapidly, leading to an increase in surface roughness due to the non-uniform formation of the oxide layer (Jun *et al.,* 1995). This roughness is attributed to the uneven oxide development across different crystal orientations or microstructural features present on the Si surface.

After a certain period, the oxidation rate diminishes as the oxide layer becomes thicker. This reduction is primarily attributed to the diffusion-limited nature of the oxidation process, where oxygen molecules or oxidizing species must diffuse through the already-formed oxide layer to reach the underlying substrate. As the oxide layer grows, the diffusion pathway lengthens, reducing the rate at which oxidation occurs.

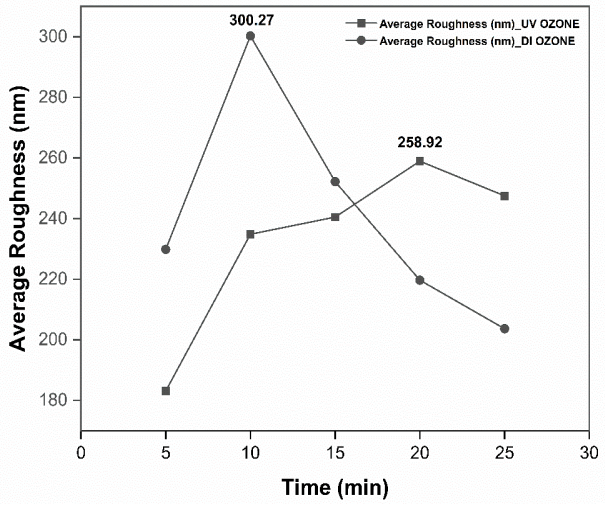

Fig 2. Average roughness of wafer surfaces according to the ozone treatment

This self-limiting behavior results in a more uniform surface as the oxidation process stabilizes and progresses consistently across the substrate. Thickness variations in the oxide layer can initially lead to non-uniform growth rates. However, over time, the process inherently compensates for these irregularities as thicker regions experience slower oxidation due to the extended diffusion path, while thinner regions oxidize more rapidly. This dynamic contributes to surface smoothing by gradually covering the initial irregularities and creating a consistent oxide layer across the substrate.

Prolonged or excessive exposure to ozone treatment may result in surface oxidation, roughening, and possible structural impairment of the Si wafer, which could be potentially harmful, depending on the application (Bakhshi *et al.,* 2018). Moreover, prolonged exposure can result in excessive oxidation, forming a thicker-than-desired silicon oxide layer (Özçam *et al.,* 2014). With prolonged treatment durations, the oxide layer becomes more uniform as it consistently covers both high and low areas on the surface. This "filling in" contributes to a decrease in the overall surface roughness. Initially, treatments with UVO_3 or DIO_3 result in an increase in the roughness of the Si surface due to rapid and non-uniform oxidation. However, as the oxide layer continues to thicken and attain a more uniform structure, the surface ultimately becomes smoother, achieving a stable and self-limiting thickness refers to the point at which the growth rate of the oxide layer significantly slows down due to the diffusion-limited nature of the oxidation process (Fu *et al.,* 2024). Therefore, managing the duration of ozone exposure is crucial for maximizing beneficial outcomes while minimizing potential negative effects.

3.2 X-ray diffraction analysis

The XRD analysis was conducted to determine the crystallinity of the samples, focusing on the structural integrity of the Si wafers after different cleaning processes. The analysis demonstrates a prominent peak centered at 69.1° (JCPDS file 271402), corresponding to the (400) plane of Si, which is a key indicator of silicon's crystalline structure. Fig 3 illustrates the XRD patterns for Si wafers subjected to various cleaning treatments, highlighting significant differences in crystallinity. Among the treatments, the DIO_3 cleaning process exhibits the highest peak intensity, indicating enhanced crystallinity compared to the other methods. The enhancement in crystallinity observed with DIO_3 cleaning could be attributed to its effective removal of surface contaminants and oxides, ensuring a pristine and smooth Si surface. By eliminating impurities and native oxide layers more efficiently than other methods, DIO_3 cleaning minimizes surface defects that could otherwise disrupt the alignment of Si atoms. This results in a more orderly and well-defined crystal lattice, which is crucial for semiconductor applications. Fig 3 specifically underscores the correlation between cleaning methods and the structural quality of the Si wafers, with DIO_3-treated wafers demonstrating superior crystallinity as evidenced by the intensity and sharpness of the (400) peak.

The ozone treatments primarily affect only the very top surface layer of the Si wafer by forming a thin Si oxide layer, typically a few nanometers thick. This oxidation process is considered mild since it is performed at ambient temperature, without the involvement of high temperatures, harsh chemicals, or physical abrasion, and relies solely on the reactive species generated by ozone (Fink *et al*., 2009). Since the implemented ozone treatment does not involve high temperatures or physical abrasion, the underlying crystal structure of the silicon remains mostly unaffected. It refers to a negligible structural impact on

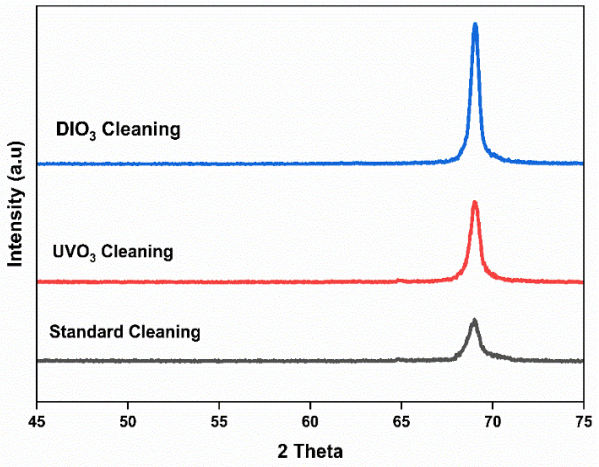

Fig 3. XRD patterns of the different cleaning process of silicon wafer for standard cleaning, 20-min UVO_3 and 10-min DIO_3

the underlying crystal lattice of the silicon. While the surface undergoes oxidation, the bulk silicon retains its original crystalline structure, as the ozone treatment does not introduce thermal stress or induce significant changes beyond the surface oxide formation. This ensures that the intrinsic properties of the silicon wafer remain intact, preserving its suitability for high-precision applications. Moreover, the amorphous nature of the oxide layer ensures compatibility with subsequent processing steps, as it forms a uniform and defect-free barrier.

The XRD pattern presented in Fig 4 reveals that the peak intensity increases when two-step textured wafers are subjected to the DIO_3 cleaning process. This enhancement in intensity suggests that DIO_3 cleaning contributes to higher crystallinity by removing surface contaminants and native oxides more effectively, thereby exposing and preserving the intrinsic crystalline structure of the Si substrate. In contrast, the samples cleaned using standard cleaning and UVO_3 methods exhibit a reduction in XRD intensity. This reduction may be attributed to less effective cleaning, which leaves residual contamination or uneven oxide layers that interfere with the structural regularity of the Si surface. The correlation between surface morphology and crystallinity is further supported by the analysis of Fig 8(e), which displays the surface morphology of the samples. The smoother and more uniform surface observed in the DIO_3 cleaned wafers aligns with the higher XRD intensity, as a well-textured, clean surface minimizes scattering and enhances the detection of crystalline planes. Conversely, the less uniform and rougher morphology of the UVO_3 and standard-cleaned wafers contributes to reduced crystallinity, as these surfaces are more prone to structural distortions and defects that degrade crystalline order.

Texturing is a more aggressive process designed to create a textured pyramid pattern on the Si surface. This process involves anisotropic etching, which preferentially removes material along specific crystal planes of silicon, typically the (111) plane, due to differences in etching rates among crystal orientations (Akila *et al.*, 2017). The result is the formation of well-defined facets with specific orientations, which enhances light trapping and reduces surface reflectivity. Ozone treatment, on the other hand, affects only the very top surface by forming a thin amorphous Si oxide layer without significantly altering the crystallinity of the Si wafer. The two-step texturing process combines the benefits of light-trapping textures from etching with the preservation of the bulk silicon's crystalline structure, ensuring that the material retains its essential properties for efficient solar cell performance.

In both the ozone and texturing processes, the bulk crystallinity of the Si wafer remains intact, which is crucial for maintaining the electrical properties required for efficient solar cell operation. Bulk crystallinity ensures the Si crystal lattice is well-ordered and free of significant defects, directly impacting charge carrier mobility. High-quality crystalline Si allows for minimal scattering and recombination of charge carriers (electrons and holes), enabling them to travel efficiently through the material to the electrodes. This high carrier mobility translates to better current flow and higher conversion efficiency in solar cells. Any disruption to the bulk crystallinity, such as the introduction of defects or amorphous regions, would result in increased recombination rates, reducing the overall performance of the solar cell.

Tables 1 and 2 provide the full width at half-maxima (FWHM), crystallite size and peak positions for various cleaning and texturization processes. FWHM refers to the width of a peak at its half-maximum intensity in an X-ray diffraction (XRD) pattern. It is a measure used to estimate the crystallite size and lattice strain in materials. A narrower FWHM corresponds to larger crystallite sizes and lower lattice strain, indicating higher crystal quality. FWHM analysis to estimate the crystallite size and detect strain in a material. Remarkably, the texturing with 10 minutes DIO_3 cleaning suggests that the FWHM does not demonstrate substantial changes, which suggests that the crystallite size is effectively constant. The size of the crystallites within a Si wafer can substantially impact its optical characteristics, particularly in light reflectance. Smaller crystallites introduce more grain boundaries, which can scatter light more effectively, increasing light absorption in textured surfaces. The anticipated crystallite sizes of the samples were consistently 80 nm across all samples, regardless of the texturing observed. This size provides a balance small enough to enhance surface interaction with light yet large enough to maintain structural stability and minimize excessive grain boundary effects. This value lies within the medium crystallite size range (10 nm – 100 nm), where there can be noticeable changes in reflectance, and the optical properties start to stabilize compared to smaller sizes (<10 nm) (Das & Sarkar, 2016).

These smaller crystallite sizes generally increase surface roughness due to more grain boundaries and irregularities,

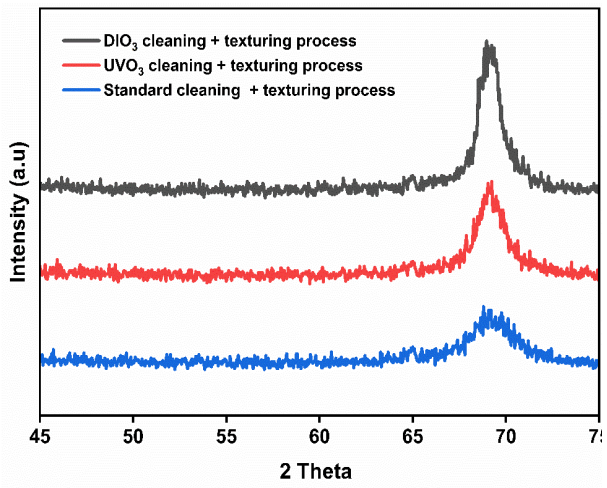

Fig 4. XRD patterns of the after-two-step texturing process of silicon wafer

Table 1
Data obtained from XRD patterns for different cleaning process

Sample	FWHM (2 Theta)	Crystallite Size (nm)	Peak Position (2 Theta)
Standard cleaning	0.81	80.66	69.17
UVO_3 cleaning	0.65	142.51	69.17
DIO_3 cleaning	0.53	169.68	69.17

Table 2
Data obtained from XRD patterns after texturing process

Sample	FWHM (2 Theta)	Crystallite Size (nm)	Peak Position (2 Theta)
Standard cleaning + Texturing process	1.25	78.41	69.17
UVO_3 cleaning + Texturing process	1.29	77.83	69.17
DIO_3 cleaning + Texturing process	1.32	76.09	69.17

especially in crystalline Si (Khanna *et al.,* 2015). For solar cell applications, achieving an optimal pyramid size and roughness is key to balancing light trapping (Park et al., 2020).

The data presented in Section 3.2 reveal that the DIO_3-treated wafers achieved a consistent crystallite size of approximately 80 nm across different texturing durations, with minimal changes in FWHM. This result indicates that the treatment maintains the structural integrity of the Si surface while allowing for effective texturing. The textured surfaces demonstrated uniform pyramid structures with dimensions conducive to effective light trapping. Moreover, the roughness introduced by the texturing process aligns well with the medium crystallite size, ensuring reduced reflectance and enhanced absorption. The balance between surface roughness and crystallite size achieved through the DIO_3 process is a key outcome. This is attributed to the fact that it supports the creation of efficient light-trapping structures while preserving the electrical properties of the underlying silicon. This highlights the effectiveness of DIO_3 cleaning in maintaining an optimal surface morphology for solar cell performance.

3.3 Spectral reflectance analysis

The enhancement of minority carrier lifetime and photoelectric conversion efficiency in monocrystalline Si solar cells is notably achieved through the reduction of optical reflectance, which allows for the capture of increased incoming light (Kegel *et al.*, 2013). The reflectance data depicted in Fig 5 corresponds to the variations in UVO_3 cleaning time. Optical reflectance for the wafers diminishes with increasing wavelength up to 600 nm while maintaining relative constancy between 600 and 1000 nm, as displayed in Fig 5 (a). The wafers treated with 20 minutes of UVO_3 demonstrate the lowest

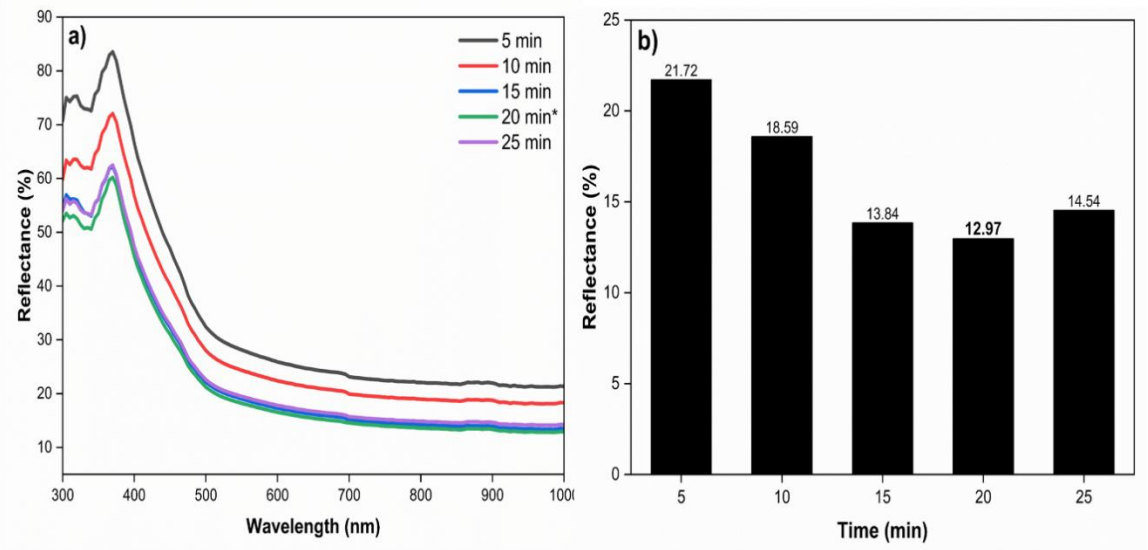

Fig 5. (a) Reflectance spectrum of UVO_3 samples and (b) minimum percentage of reflectance values with different time of UVO_3 cleaning process

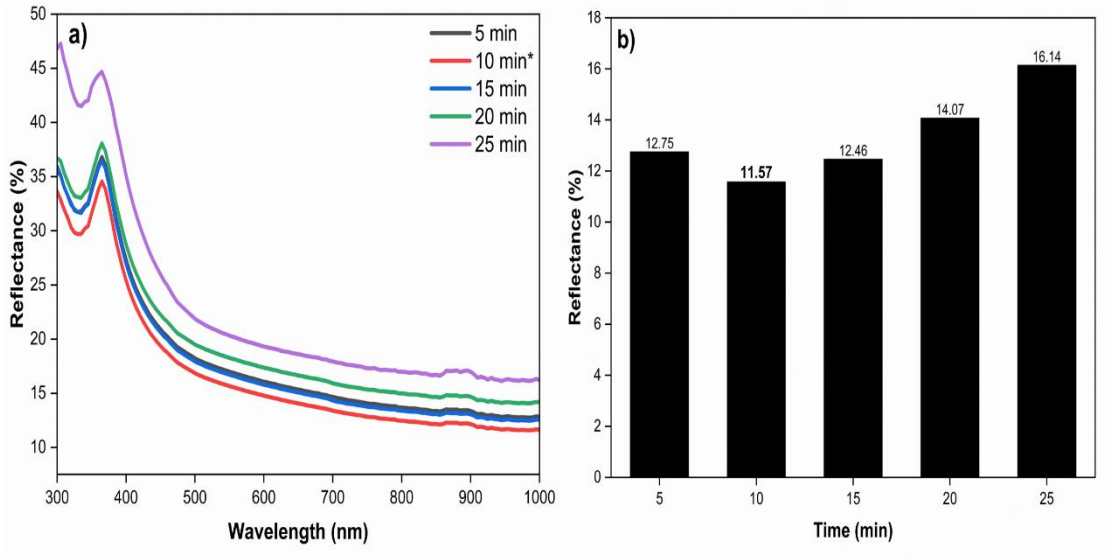

Fig 6. (a) Reflectance spectrum of DIO_3 samples and (b) minimum percentage of reflectance values with different time of DIO_3 cleaning process

reflectance (12.97%), which is in good agreement with the large surface roughness of the samples.

The presence of significant surface roughness can enhance the light-trapping capabilities of the textured surface (Fashina *et al.*, 2018). Despite that, the reflectance of wafers starts to increase after being subjected to 25 minutes, where the wafers exhibit a reflectivity of 14.54%. The analysis of AFM images for samples subjected to 5 minutes of UVO_3 treatment Fig 1 (b)(i) reveals significant non-etched regions and a relatively low surface roughness on the wafer's surface, which diminishes the wafers' capacity for effective light trapping. Fig 5(a) illustrates the AFM image of a wafer subjected to 5 minutes of UVO_3 treatment. The image highlights a surface characterized by significant non-etched regions with a relatively low surface roughness. The surface appears smoother, with fewer pronounced peaks and valleys compared to samples subjected to longer treatment times. This lack of surface texturing reduces the wafer's ability to trap light effectively, thereby diminishing its optical performance. The comparison between Fig 5(a) and other AFM images emphasizes the importance of achieving adequate surface roughness through optimized treatment durations. Insufficient etching, as observed here, can lead to higher reflectivity and lower light absorption, which are detrimental to the performance of solar cells.

Fig 6 indicates the reflectance measurement of Si wafers textured by different DIO_3 time processes as a function of wavelength. According to Fig 6 (b), the wafers subjected to the two-step texturing process with 10 minutes of DIO_3 cleaning treatment demonstrate the smallest surface reflectance (11.57%) compared to other time processing. The results demonstrate that superior anti-reflection properties are attained by utilizing small pyramid dimensions, ensuring effective surface coverage, and maintaining a uniform and homogeneous arrangement of the pyramids, as depicted in Fig 8 (e) (Al-Husseini & Lahlouh, 2019).

The correlation between the surface roughness and the reflectance of each wafer is presented in Fig 7. The two-step texturing process with 10 minutes of DIO_3 cleaning time yields wafers with the highest value of average roughness (300.27 nm)

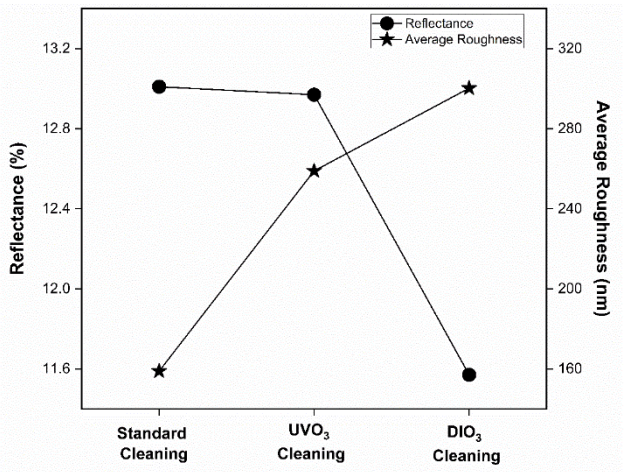

Fig 7. Average roughness and reflectance of wafer surfaces according to the cleaning process

and the lowest reflectance value (11.57%). The result is anticipated to enhance the efficacy of solar cells.

The presence of significant surface roughness can enhance the light-trapping capabilities of the textured surface (Fashina et al., 2018). However, the reflectance of wafers increases after 25 minutes of treatment, reaching a reflectivity of 14.54%. The analysis of AFM images for samples subjected to 5 minutes of UVO_3 treatment reveals significant non-etched regions and relatively low surface roughness on the wafer's surface, which diminishes the wafers' capacity for effective light trapping. Fig 7 illustrates the relationship between the surface roughness and the reflectance of each wafer. The two-step texturing process with 10 minutes of DIO_3 cleaning time yields a wafer with the highest value of average roughness (300.27 nm) and the lowest reflectance value (11.57%). The result is anticipated to enhance the efficacy of solar cells.

3.4 Microstructure on different textured wafers

Fig 8 (a, c and e) presents the FESEM images of textured Si wafer surfaces subjected to different cleaning methods. Fig 8 (b, d and f) represents pyramid facets obtained from the cross-section of the samples. In general, a random pyramidal structure was successfully developed on all samples, signifying the ability of each approach to be employed as a cleaning method. This micrograph indicates that the ozone-cleaning process can significantly enhance the texturing process for Si wafers by modifying the surface properties (Gao, 2021). During the texturing process, the Si wafer is often treated to create a pyramidal structure that increases light absorption (Zhang *et al.,* 2021).

The ozone cleaning procedure does not directly influence the dimensions of the pyramids formed on a Si wafer. Instead, it serves to maintain a clean and uniform surface on the Si wafer, eliminating organic contaminants and particles that may lead to irregular texturing. A uniform surface is essential for ensuring uniform pyramid dimensions throughout the wafer, as any contamination may lead to defects or discrepancies in the size of the pyramids. The size of the pyramids is predominantly influenced by the texturing process, which is contingent upon the crystal orientation of the Si wafer. In this study, the texturing process has been refined based on previously reported findings (K & O, 2023; Raji *et al*., 2022).

Following the texturing process, the intercept method was employed to determine the size of the pyramid (Park et al., 2009). The intercept method is to draw diagonal lines on the FESEM image and count the number of diagonal pyramids. The number of pyramids intersecting the line is counted. The average pyramids are determined by dividing the number of intersections by the actual line length.

As a result of the measurement, the pyramid size of the textured sample with standard cleaning is 4.3–4.6 µm, UVO_3 cleaning 3.2–3.3 µm, and DIO_3 cleaning 1.9–2.0 µm. The findings after ozone cleaning distinctly indicate that the surface condition prior to texturing influences the development of the pyramid structure. Furthermore, following the DIO_3 cleaning process, a more consistent pyramid shape can be observed. As depicted in Fig 8 (b, d, and f), the pyramidal development resulting from the DIO_3 cleaning process is considerably more substantial than the standard and UVO_3 process. Furthermore, the size of the pyramids generated through DIO_3 is the smallest when compared to the other cleaning processes.

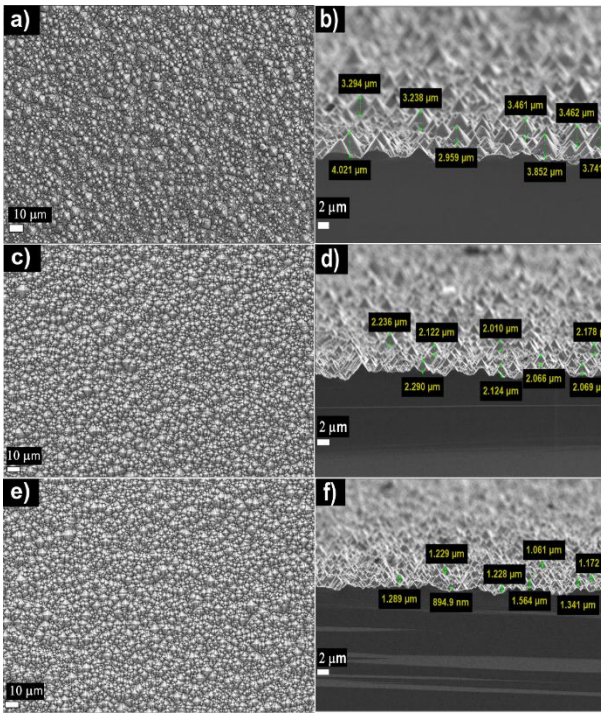

Fig 8. FESEM micrographs of Si surface and variation of pyramid height after textured for different cleaning process: (a & b) standard cleaning, (c & d) UVO_3 cleaning and (e & f) DIO_3 cleaning

Ultimately, the adoption of DIO_3 treatment plays a crucial role in improving the efficiency of textured Si wafer manufacturing by facilitating comprehensive cleaning and oxidation and ensuring uniformity in the etching process. This process ultimately results in the attainment of the desired pyramid size, thereby enhancing performance while reducing the time required for cleaning. Compared to the traditional RCA washing method, DIO_3 uses fewer chemicals while delivering superior results. Additionally, the DIO_3 process reduces chemical usage costs and improves the performance of solar cells, making it a more efficient and cost-effective solution.

4 Conclusion

This study has effectively demonstrated a viable cleaning method for texturizing the surfaces of p-type Si wafers through a two-step texturing procedure. The DIO_3 cleaning process results in the formation of pyramidal structures of varying sizes, enhancing the efficacy of surface texturization. A 10-minutes DIO_3 cleaning process obtained a good time for creating the surface with a homogenous and uniform pyramidal size, where the lowest surface reflectance was discovered at 11.57%. The average pyramid size and height were 1.9 µm and 1.2 µm, respectively. Therefore, the implementation of the DIO_3 cleaning process, as detailed in this research, presents a viable approach for developing a simple, cost-effective, and non-toxic solar cell that exhibits improved conversion efficiency.

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Conflicts of interest
The authors declare no conflict of interest

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